Amendments to the Specification:

Please replace the paragraph at page 7, lines 23-24 with the following amended paragraph:

FIGS. 9A through [[9H]] 9I show main waveforms of operation of the data latch shown in FIG. 8;

Please replace the paragraph at page 18, lines 11-20 with the following amended paragraph:

FIGS. 9A through [[9H]] 9I show main waveforms in the operation of the data latch shown in FIG. 8. FIG. 9A shows the first non-overlapping clock signal CKP0. FIG. 9B denotes channel data of nine bits input to the first latch 710. FIG. 9C shows the first latch clock signal CKL1 for controlling the operation of the first latch 710. FIG. 9D shows channel data latched by the first latch 710. FIG. 9E shows a second latch clock signal CKL2 for controlling the operation of the second latch 720. FIG. 9F shows the channel data latched by the second latch 720. FIG. 9G shows a third latch clock signal CKL3 for controlling the operation of the third latch 730. FIG. 9H shows the channel data latched by the third latch 730. FIG. 9I shows the result of serializing the data latched by the data latch shown in FIG. 8 by the data serializer 750 (refer to FIG. 6).